

A Frequency Dispersion Model of GaAs MESFET for Large-Signal Applications

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Abstract— Deficiencies in conventional frequency dispersion models of GaAs MESFET are addressed regarding their large-signal response. A new model which can accurately describes the large-signal dynamic properties is proposed. Only dc and scattering parameter data are required to extract the model parameters, which can be easily implemented into microwave circuit simulators in the macro circuit form. The validity of this model is demonstrated by comparing predicted pulsed I-V characteristics and power saturation characteristics with measured ones.

Index Terms—Empirical method, MESFET's, nonlinear model, power amplifier, semiconductors, S-parameter measurements.

I. INTRODUCTION

GAAS MESFET's fabricated based on current technologies show low-frequency dispersion in their transfer and output characteristics. These are known to be due to traps and self-heating effects [1], [2], have been an obstacle to model-based circuit design. Various empirical models have been proposed to model the discrepancy of dc and small signal RF conductance [3]–[5]. Some of large signal models show excellent fitting of dc and scattering parameters over wide bias range. Therefore, one might expect that the accuracy will be preserved when these models are used to predict high-frequency large-signal responses. However, this is unfortunately not true. Fig. 1 presents one example for the failure of models. The pulsed I-V characteristics are simulated with EEFET3 model in Libra, whose model parameters were extracted by EESof-Xtract based on scattering parameters measured from 0.5 to 6 GHz and dc I-V characteristics. The simulated traces show failure of turn-off below threshold region and at zero drain voltage. The amount of this unphysical current is dependent on the bias.

This failure causes significant errors in the estimation of output power and power conversion efficiency, which may be fatal to high-efficiency power amplifier design. The above failures are found in the other frequency dispersion models, which have high-pass circuit branched to I_{ds} current source to compensate the conductance discrepancies due to the frequency dispersion. These include EEFET3, HP-Root, TOM (Triquint Own Model) in Libra [6], and some models employing a simple series resistor–capacitor circuit, as in the work of Camacho–Penalosa [7]. To avoid these failures, some circuit designers utilize pulsed I-V curve to explain the dynamic characteristic rather than frequency dispersion models [8].

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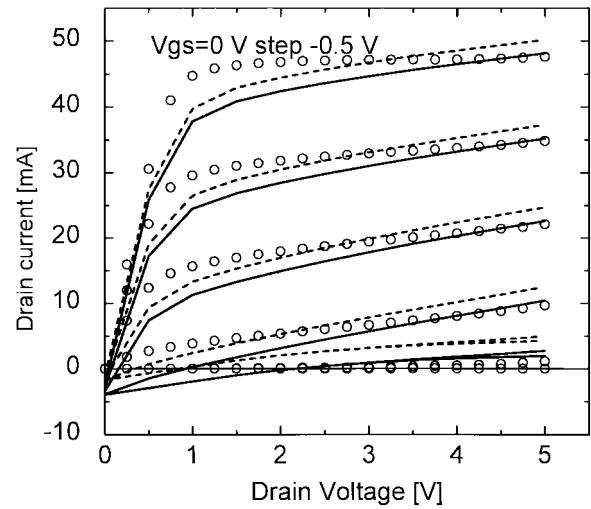


Fig. 1. Pulsed I-V characteristics simulated with EEFET3 in HP-EESofLibra. The pulse biases are $V_{ds} = 2.5$ V, $V_{gs} = -1$ V (dashed lines); $V_{ds} = 4$ V and $V_{gs} = -1.5$ V (solid lines). I-V traces show failure of turn-off even below threshold ($V_{gs} = -2.5$ V) and do not cross zero at $V_{ds} = 0$ V. Hollow circles are dc I-V characteristics.

However, since the pulsed I-V depends on bias point, the bias of the measurement should be coincided with the bias of the circuit to be designed. To fit dc I-V and bias-dependent pulsed I-V simultaneously, various approaches have been proposed. These include the look-up table approach in [9] and effective gate-source potential approach [10]. However, this method does require unconventional measurement setup [11]. Hence, a frequency dispersion model has been needed for large signal circuit design, which is accurate and easy to implement and extract model parameters. In this letter, we introduce simple modeling scheme that can utilize existing large signal models while requiring only dc and S parameter data. Despite its simplicity the proposed model avoids deficiencies mentioned above.

II. MODEL

The modeling scheme is composed of following two procedures. The one is fitting the existing model to dc I-V and the other is determining α_1 and α_2 (to be explained later) fit best scattering parameters measured at the frequency far above the dispersion transition occurs. Let f be the function describing dc drain-source current of a certain large signal model and device terminal voltages be the input variables

$$I_{ds} = f(V_{gs}, V_{ds}). \quad (1)$$

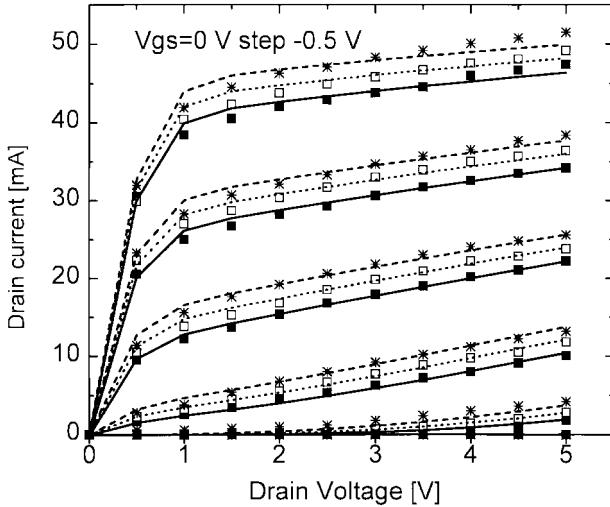


Fig. 2. Predicted pulsed I-V's by proposed scheme and measured ones at three different biases. Line traces are the simulated and scattered points are the measured. Bias of pulse measurements are $V_{ds} = 2.5$ V and $V_{gs} = -1$ V (dot lines and open square); $V_{ds} = 4$ V and $V_{gs} = -1.5$ V (solid lines and solid square); $V_{ds} = 2$ V and $V_{gs} = 0$ V (dashed lines and stars). The model parameters are $\alpha_1 = 0.031$ and $\alpha_2 = 0.947$.

Note that f describes just dc drain-source current in (1). To extend the usage of f to rf, some modifications of f are required. The proposed scheme just replaces the first argument V_{gs} with

$$V_{gsX} = \bar{v}_{gs} + \alpha_1(v_{ds}(t) - \bar{v}_{ds}) + \alpha_2(v_{gs}(t) - \bar{v}_{gs}) \quad (2)$$

where \bar{v}_{gs} and \bar{v}_{ds} are the static component of time varying terminal voltages of $v_{gs}(t)$ and $v_{ds}(t)$. This replacement results in new model function

$$i_{ds}(t) = f(V_{gsX}, v_{ds}(t)). \quad (3)$$

In dc operation, the contribution of α_1 and α_2 are zero since $v_{ds}(t) = \bar{v}_{ds}$ and $v_{gs}(t) = \bar{v}_{gs}$. In rf operation, α_1 performs the output conductance dispersion by feeding dynamic component of drain signal back to the gate and α_2 the transconductance dispersion by weighting dynamic component of gate signal without disturbing each other. The parameter α_1 has already been employed in the previous attempt to model pulsed I-V and its bias dependency [11]. This modification does not alter the properties of f in (1), such as "zero-crossing" at zero drain voltage or "turn-off" characteristic at the threshold region. Thus, new model function in (3) avoids failures discussed with Fig. 1 as existing dc I-V functions do.

After fitting EEFET3 to DC I-V, the two parameters (α_1 and α_2) are extracted through optimization to measured S parameters of multi-bias points in saturation region. Points are selected so that they cover operating region. After optimization resultant average S parameter error was 5% with maximum of 10% in 16 points equally spaced with respect bias voltage. With new model, we get the improved results as in Fig. 2. Pulsed I-V characteristics are simulated with optimized parameters $\alpha_1 = 0.031$ and $\alpha_2 = 0.947$. The measurements were done at three different bias points: $V_{ds} = 2.5$ V, $V_{gs} = -1$ V; $V_{ds} = 4$ V, $V_{gs} = -1.5$ V; $V_{ds} = 2.0$ V and $V_{gs} = 0$ V. A series of pulses of 1 μ s width with 0.001 duty were

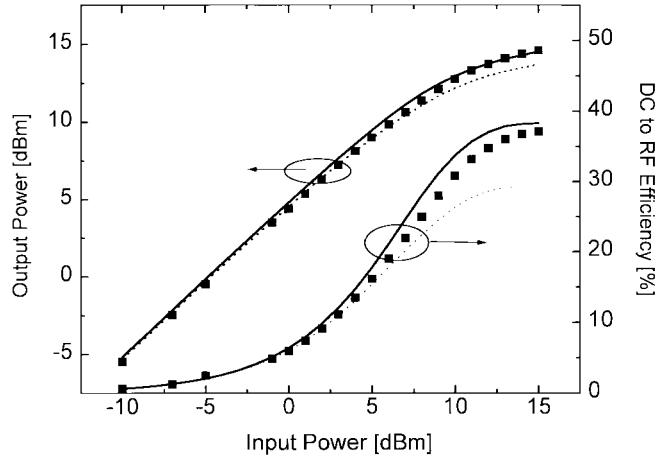


Fig. 3. P_{in} - P_{out} characteristic and dc-to-rf efficiency at drainin 50- Ω terminated amplifier at 100 MHz. Square points are measured ones, solid lines are simulated with proposed scheme applied to EEFET3, and dot lines are simulated with EEFET3 without modification.

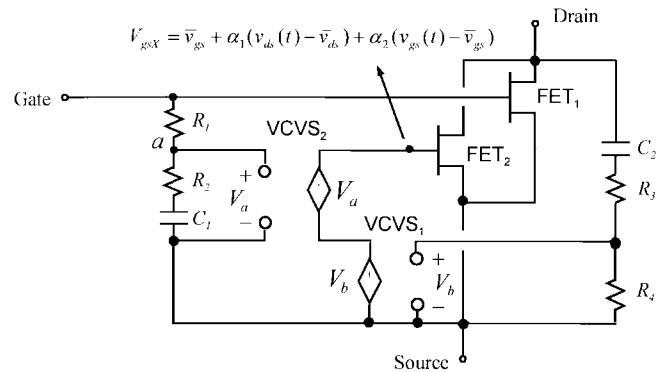


Fig. 4. The macro circuit realizing the proposed scheme using two partial FET models and linear elements.

applied to both gate and drain simultaneously. Measurements were carried out using specially designed on-wafer pulse I-V system. In this figure, one can see a clear "turn-off" at sub-threshold region and "zero-crossing" at zero drain voltage in both measured and simulated characteristics. It is worthwhile to note that the model predicts also the bias dependency of pulsed I-V characteristics.

On the tested FET, P_{out} - P_{in} characteristics are measured in 50- Ω terminated condition at 100 MHz. The results are plotted with predicted ones in Fig 3. The harmonic-balance simulations are done with proposed scheme and EEFET3. In the small-signal region EEFET3 does slightly better prediction. However, as power saturates, EEFET3 brings significant errors in efficiency and output power calculation.

Owing to the simplicity of the model, circuit level implementation is possible by the exploiting dc part of existing models. The macro circuit of Fig. 4 is an example. FET₁, which has its drain current source disabled, plays the role of the conduction path of gate current. On the other hand, FET₂, which has only the drain current source, does the complement role of FET₁. Two FET's are merged into one complete FET. Resistor-capacitor circuits and two voltage-controlled voltage source (VCVS's) realize the (2). R_1 , R_2 , and C_1 determines

α_2 and the transition frequency of transfer dispersion. In this network \bar{v}_{gs} is directly coupled to node a . At high frequency, since C_1 acts as an effective short, node a sees the voltage of $\bar{v}_{gs} + \alpha_2(v_{gs}(t) - \bar{v}_{gs})$, where α_2 is the voltage-dividing ratio $R_2/(R_1 + R_2)$. The time constant of $C_1(R_1 + R_2)$ is set to have about 1 ms, as is quite common in other equivalent circuit approach of frequency dispersion model. A similar explanation can be made for R_3 , R_4 , and C_2 . R_3 and R_4 determines α_1 , and C_2 blocks static component of drain signal. The two series-connected unity-gain VCVS's apply the sum of voltages: $\bar{v}_{gs} + \alpha_2(v_{gs}(t) - \bar{v}_{gs})$ and $\alpha_1(v_{ds}(t) - \bar{v}_{ds})$ to the gate of FET₁. R_1 , R_2 , R_3 , and R_4 should be high enough so that we can neglect the current pass through them. All additive elements in Fig. 4 (resistors, capacitors, and VCVS's) are available in most of modern circuit simulators.

III. CONCLUSION

We addressed deficiencies found in conventional frequency dispersion models of large signal models for GaAs MESFET. To fix this problem we propose a very simple modeling scheme that accurately predicts the large signal responses. It can be easily combined to existing empirical models in the macro circuit form. The validity of this model is shown by comparing measured and simulated results for multi-bias pulsed I-V characteristics and P_{out} - P_{in} characteristic of the device. This model is shown to result in better estimation of output power and dc-to-rf power conversion efficiency.

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